

REMARKS

Applicant notes, with appreciation, the indicated allowability of Claims 32-40, 55 and 56.

Claims 1-31,41-54 have been rejected under 35 U.S.C. 102(e) as being anticipated by Heaslip et al. US-Patent 6,643,807 issued on November 4, 2003 and filed on August 1, 2000. Applicant has carefully reviewed Heaslip et al. and believes that it fails to meet the well established test for anticipation. Accordingly, favorable reconsideration is respectfully requested in light of the following comments.

The present invention seeks to provide a method and test controller for transferring memory failure information off-chip at a tester clock rate while performing a memory test at a system clock rate. The method of the present invention is a continuous process in that it is not necessary to stop the method or controller to permit failure information to be scanned out of the chip. This is reflected in method claim 1 which requires "selectively generating a failure summary on-circuit while performing said testing; and transferring said failure summary from said circuit under control of a second clock concurrently with testing of the next column or row in sequence" (emphasis added). Clearly, the method is not stopped to unload failure information. It will also be noted that testing is performed at a first clock rate. This would be the system speed of the memory. The transferring of the failure summary off-chip is at a second clock rate. This is the tester speed.

It will also be seen that the method generates a "failure summary". As taught in the specification, the failure summary contains information about several failures occurring within a row or a column under test.

Claims 2-40 depend from claim 1 and, therefore, also include the features of claim 1. Similar comments apply independent claim 41 and its dependent claims 42-54.

FIG. 2 of Heaslip is a flow diagram which illustrates a preferred method of the Heaslip invention. The figure clearly shows that if a failure is detected at step 35, the method proceeds to step 36 where the method is stopped and data is scanned out. The stopping of the BIST controller in Heaslip is described throughout the description and there is no teaching or suggestion of an embodiment in which the controller is not stopped, let alone disclosing the method of claims 1-40 and the test controller of claims 41-54. Clearly, then, Heaslip cannot be an anticipation of the claims under consideration.

Furthermore, Heaslip neither discloses nor remotely suggests scanning out a "failure summary" which could contain information about several failures in a row or column. In Heaslip, the BIST engine stops only (sic) at each failed cycle. So, not only does Heaslip have to stop to scan out the contents of various registers of the BIST engine, he also has to scan out those registers more often because he stops at each failed cycle. This is contrary to the present invention. Note also that Heaslip's method focuses on exact diagnosis of each failure. In the method of the present invention, the exact location of every failure might not be known --- it is sufficient to know the approximate location for the purposes outlined in the summary of the invention: "The present invention seeks to provide a method of collecting memory failure information in real time for memories tested using an embedded memory test controller for the purpose of process monitoring, yield enhancement, redundancy analysis and bitmap generation."

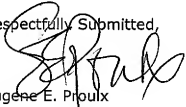
As the Examiner is well aware, a claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or

Inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

It is clear from the foregoing that the applied reference fails to disclose each and every element of the claims against which the reference has been applied. Accordingly, the claims must be considered novel over the reference.

It is believed that the application is in condition for allowance. Early favorable reconsideration and action to this end is respectfully requested.

Respectfully Submitted,



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